Code No: **19ECT406** **R19**

II B. TECH II SEMESTER REGULAR EXAMINATIONS, AUG/SEPT 2021
DIGITAL ELECTRONICS
(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 60

Note: Answer **ONE** question from each Unit (**5 × 12 = 60 Marks)**

UNIT - I

1.	a)	Represent $(141)_{10}$ in binary, octal and hexadecimal formats.	[4M]
	b)	What do you mean by self complementing code? What are weighted and non-weighted codes? Explain with examples.	[8M]
		(OR)	
2.	a)	Subtract $(14)_{10}$ from $(46)_{10}$ using 2's complement method.	[6M]
	b)	Explain about error detecting and correcting codes.	[6M]
		UNIT – II	
3.	a)	Explain in detail about standard SOP and POS forms with examples.	[6M]
	b)	Obtain minimal SOP expression for the Boolean function using K-map $F(W, X, Y, Z) = \Sigma m(4, 5, 9, 13, 15) + \Sigma d(0, 1, 7, 11, 12)$	[6M]
		(OR)	
4.	a)	Reduce the following function using K-map $F(A,B,C,D) = \prod M(0,2,3,8,9,12,13,15)$	[6M]
	b)	Simplify the Boolean expression using QM - tabulation method. $F(A,B,C,D) = \Sigma\, m(2,4,6,8,9,10,12,13,15)$	[6M]
		UNIT – III	
5.	a)	Design full subtractor and implement using two 4:1 multiplexers.	[6M]
	b)	Implement the following Boolean function $F(X,Y,Z) = \Sigma\, m(0,2,6,7)$ with 8:1 multiplexer.	[6M]
		(OR)	
6.	a)	What is a full adder? Give its truth table. Derive logic expressions for sum and carry and implement using NAND gates only.	[6M]
	b)	Construct a 4 to 16 line decoder with five 2 to 4 line decoders with enable.	[6M]
		UNIT –IV	
7.	a)	Explain briefly about different types of flip-flops.	[6M]
	b)	Design a 4-bit synchronous upcounter using JK flip-flops.	[6M]
		(OR)	
8.	a)	Design a conversion of JK flip-flop to SR flip-flop logic.	[6M]
	b)	Explain the operation of a Twisted ring counter.	[6M]
		UNIT –V	
9.	a)	Explain about Moore machine model.	[6M]
	b)	Explain the operation of serial binary adder.	[6M]
		(OR)	
10.	a)	Differentiate between the Melay and Moore Machines	[5M]
	b)	What is FSM ? Explain its components.	[7M]

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